REMARKS

The Office Action mailed November 12, 2004 has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

No extension of time is believed to be required based upon the filing of this Amendment prior to the deadline of the three-month statutory period, which is February 14, 2005 under 37 C.F.R. § 1.7 since the formal deadline falls on a Saturday. A Fee Transmittal and a credit card payment form accompanies this Amendment for covering the fee ($600.00) for excess independent claims over three. Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 024016-00063**, for any additional fees necessary for entry of this Amendment.

Claims 1, 3, 5-7 and 11 have been amended and claims 2, 4 and 14-21 have been canceled. Applicant submits that the amendments made herein are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Accordingly, claims 1, 3 and 5-12 are pending in the present application and are respectfully submitted for reconsideration.

Dependent claims 3 and 20 stand objected to for informalities. Claim 3 has been amended in response to the Examiner's objection. In addition, claim 20 has been canceled, and thus the objection with respect to this claim is moot. The objections are respectfully traversed and reconsideration is requested.

Dependent claims 15 and 16 stand objected to as being dependent upon a rejected base claim, and further stand objected to on the ground that the prior art of record fails to teach or

fairly suggest a clock multiplication circuit comprising the initial integrated value acquisition means claimed. Claims 15 and 16 have been canceled, and thus the objections with respect to these claims are moot. The objections are respectfully traversed and reconsideration is requested.

Dependent claims 20 and 21 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 20 and 21 have been canceled, and thus the rejections with respect to these claims are moot. The rejections are respectfully traversed and reconsideration is requested.

Claims 1-12, 14 and 17-21 rejected under 35 U.S.C. § 102(b) as being anticipated by the Kokubo et al. patent (U.S. Patent No. 5,982,208). Claims 2, 4 and 14-21 have been canceled, and thus the rejections with respect to these claims are moot. Independent claim 1 has been amended to include the content of dependent claim 2. In addition, dependent claims 3, 5-7 and 11 have been rewritten in independent form including much of the content of previously presented independent claim 1. Dependent claims 8-10 and 12 depend from independent claims 7 and 11, respectively. The rejections are respectfully traversed and reconsideration is requested.

Independent claim 1, as amended, recites a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising, in part, a counter wherein the counter is a counter for delivering the count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is at either a High level or a Low level, the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics such that when the count value is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the counting period and before the start of a succeeding counting

period. Applicant respectfully submits that the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit as claimed in the present invention.

The Kokubo et al. patent discloses a clock multiplier that controls the frequency of an output clock signal (fout) according to the frequency of an input clock signal (fref) by means of switching between two feedback loops. With reference to Fig. 4, the clock multiplier disclosed merely continuously counts an output clock signal (fout) by taking, as one cycle, both a High level period and a Low level period of the input signal (fref) corresponding to the reference clock signal SR of the invention. (col. 3, ls. 13-22)

In contrast, the counter of the present invention counts an output clock signal ST when a reference clock signal SR is at either a High level or a Low level. In other words, the output clock signal ST is counted only when the reference clock signal SR is at a High level or only when it is at a Low level. Based on a result counted during the (first) High level period, the frequency of the output clock signal ST is changed before the start of a succeeding (second) High level period following a Low level period after the (first) High level period. Accordingly, the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit as claimed in the present invention. Even were the output of accumulator register 18 (Fig. 11) switched, the Kokubo et al. patent fails to disclose or suggest how long the output (control voltage) Vr of low pass filter (LPF) 4 delays changing, and thus fails to disclose the response characteristics of the circuit shown in Fig. 11.

Independent claim 3, as amended, recites a clock multiplication circuit comprising, in part, a counter wherein the counter is a counter for obtaining the count value at end of every High level period and every Low level period. As argued above, the Kokubo et al. patent merely discloses that the output clock signal (fout) is counted by taking both the High level period and

the Low level period as one cycle. Thus, the Kokubo et al. patent does not disclose or suggest the clock multiplication circuit as claimed in the present invention.

Independent claim 5, as amended, recites a clock multiplication circuit comprising, in part, a counter wherein the counter delivers the count value after the end of the counting period and in synchronization with the output clock signal, the subtracter delivers the difference value after the end of the counting period and in synchronization with the output clock signal, and the control voltage generation circuit delivers the analog control voltage after the end of the counting period and in synchronization with the output clock signal.

In contrast, in the Kokubo et al. patent, the counter does not output a count value Nv in sync with the output clock signal (fout). Rather, with reference to Fig. 4, the counter outputs the count value Nv at a falling time (edge) of the reference clock signal (fref). When the count value Nv is outputted at the falling time of the reference clock signal (fref), a comparator immediately outputs a signal CMP (1 or 0) and successively the output of the register 8 is updated. Further, the Kokubo et al. patent does not disclose the operation timing of subtracter 17 and accumulator register 18. Accordingly, the Kokubo et al. patent fails to disclose or suggest the content recited.

Independent claim 6, as amended, recites a clock multiplication circuit comprising, in part, a counter wherein both rising edges and falling edges of the output clock signal are taken as the effective transition edges by the counter. For the same reasons set forth with respect to claim 5, it is submitted that the Kokubo et al. patent does not disclose counting at each of the rising edge and the falling edge of the output clock signal.

Independent claim 7, as amended, recites a clock multiplication circuit comprising, in part, a control voltage generation circuit wherein a multiplier for multiplying the difference value by a predetermined factor and delivering a multiplied difference value to the control voltage

generation circuit is interposed between the subtracter and the control voltage generation circuit. The Examiner has noted in the Office Action that the controller 10 and the accumulator register 18 of the Kokubo et al. patent correspond to a multiplier. However, the controller 10 is merely used to switch switches SW1 and 2 or to initialize the register 8 (col. 2, l. 65 – col. 3, ls. 48-67, and col. 4, ls. 26-38). The Kokubo et al. patent does not disclose any description about a multiplying function as the multiplier, or that the accumulator register 18 may be regarded as a shift register.

Independent claim 11, as amended, recites a clock multiplication circuit comprising, in part, a subtracter for delivering a difference value obtained by subtracting either the count value or a reference value from the other, wherein the subtracter is capable of switching the reference value. The Kokubo et al. patent does not disclose any of Figs. 4 and 11 that reference value is N, which can be changed to a different value. Thus, the Kokubo et al. patent fails to disclose or suggest the content recited.

In addition, the Kokubo et al. patent also does not disclose the content of dependent claims 9 and 10, namely, that the factor of the multiplier is a variable. Indeed, the Kokubo et al. patent includes no disclosure that the accumulator register 18 has the multiplying function as the multiplier. Further, the Kokubo et al. patent also does not disclose the storage means of the subtractor as claimed in dependent claim 12. Rather, the element 11 in the Kokubo et al. patent is an internal counter 11, which does not store the reference value N.

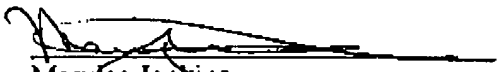
Based upon the forgoing, Applicant respectfully submits that each and every element recited within independent claims 1, 3, 5-7 and 11 are neither disclosed nor suggested by the Kokubo et al. patent, and are therefore patentable and in condition for allowance. Reconsideration is requested.

It is further submitted that dependent claims 8-10 and 12 are also patentable and in condition for allowance due to their dependency upon independent claims 7 and 11, respectively, since the dependent claims differ in scope from the corresponding parent claims. Dependent claims 8-10 depend from independent claim 7 and dependent claim 12 depends from independent claim 11, and thus are further limited to additional features of the invention. Therefore, it is respectfully submitted that the dependent claims are patentable over the Kokubo et al. patent for at least the reasons set forth above with respect to the independent claims, as well as with respect to dependent claims 9, 10 and 12. Reconsideration is requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned counsel at the telephone number, indicated below, to arrange for an interview to expedite the disposition of this application.

Dated: February 14, 2005

Respectfully submitted,



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